WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a semiconductor region of a first conductivity type;

a first insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of a second conductivity type connected to an output terminal; and

a semiconductor region of the second conductivity type formed adjacent to the source/drain region on the semiconductor region of the first conductivity type and connected to a gate of the first insulated-gate field effect transistor.

2. The device according to claim 1, further comprising a second insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of the second conductivity type connected to the gate of the first insulated-gate field effect transistor to drive the first insulated-gate field effect transistor, wherein

a distance from the source/drain region of the first insulated-gate field effect transistor to the semiconductor region of the second conductivity type is shorter than a distance from the source/drain region of

the first insulated-gate field effect transistor to the source/drain region of the second insulated-gate field effect transistor.

3. The device according to claim 2, wherein the first and second insulated-gate field effect transistors configure an output circuit and the output circuit is an output circuit of a nonvolatile semiconductor memory device.

4. The device according to claim 3, wherein the nonvolatile semiconductor memory device is of one of NAND and AND types.

5. The device according to claim 2, wherein the first and second insulated-gate field effect transistors configure an output circuit and the output circuit is an output circuit of a controller.

6. The device according to claim 5, wherein the nonvolatile semiconductor memory device is of one of NAND and AND types.

7. A semiconductor integrated circuit device comprising:

a semiconductor region of a first conductivity type;

a first insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of a second conductivity type connected to an output terminal;

a second insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of the second conductivity type connected to a gate of the first insulated-gate field effect transistor to drive the first insulated-gate field effect transistor; and

a diode using the semiconductor region of the first conductivity type as one of an anode and cathode and having the other one of the anode and cathode formed on the semiconductor region of the first conductivity type and connected to the gate of the first insulated-gate field effect transistor, wherein

a distance from the source/drain region of the first insulated-gate field effect transistor to the other one of the anode and cathode is shorter than a distance from the source/drain region of the first insulated-gate field effect transistor to the source/drain region of the second insulated-gate field effect transistor.

8. The device according to claim 7, wherein the first and second insulated-gate field effect transistors configure an output circuit and the output circuit is an output circuit of a nonvolatile semiconductor memory device.

9. The device according to claim 8, wherein the nonvolatile semiconductor memory device is of one of NAND and AND types.

10. The device according to claim 7, wherein the first and second insulated-gate field effect transistors configure an output circuit and the output circuit is an output circuit of a controller.

11. The device according to claim 10, wherein the nonvolatile semiconductor memory device is of one of NAND and AND types.

12. A semiconductor integrated circuit device comprising:

a semiconductor region of a first conductivity type;

a first insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of a second conductivity type connected to an output terminal;

a second insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of the second conductivity type connected to a gate of the first insulated-gate field effect transistor to drive the first insulated-gate field effect transistor; and

a third insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region connected to a gate thereof and a source/drain region connected to the gate of the first insulated-gate field

effect transistor, wherein

a distance from the source/drain region of the first insulated-gate field effect transistor to the source/drain region of the third insulated-gate field effect transistor which is connected to the gate of the first insulated-gate field effect transistor is shorter than a distance from the source/drain region of the first insulated-gate field effect transistor to the source/drain region of the second insulated-gate field effect transistor.

13. The device according to claim 12, wherein the first and second insulated-gate field effect transistors configure an output circuit and the output circuit is an output circuit of a nonvolatile semiconductor memory device.

14. The device according to claim 13, wherein the nonvolatile semiconductor memory device is of one of NAND and AND types.

15. The device according to claim 12, wherein the first and second insulated-gate field effect transistors configure an output circuit and the output circuit is an output circuit of a controller.

16. The device according to claim 15, wherein the nonvolatile semiconductor memory device is of one of NAND and AND types.

17. A semiconductor integrated circuit device comprising:

a semiconductor region of a first conductivity type;

a first insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of a second conductivity type connected to an output terminal;

a second insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of the second conductivity type connected to a gate of the first insulated-gate field effect transistor to drive the first insulated-gate field effect transistor; and

a bipolar transistor having a base formed of the semiconductor region of the first conductivity type, an emitter/collector region connected to the base and an emitter/collector region connected to the gate of the first insulated-gate field effect transistor, wherein

a distance from the source/drain region of the first insulated-gate field effect transistor to the emitter/collector region of the bipolar transistor which is connected to the gate of the first insulated-gate field effect transistor is shorter than a distance from the source/drain region of the first insulated-gate field effect transistor to the source/drain region of the second insulated-gate field effect transistor.

18. The device according to claim 17, wherein

the first and second insulated-gate field effect transistors configure an output circuit and the output circuit is an output circuit of a nonvolatile semiconductor memory device.

19. The device according to claim 18, wherein the nonvolatile semiconductor memory device is of one of NAND and AND types.

20. The device according to claim 17, wherein the first and second insulated-gate field effect transistors configure an output circuit and the output circuit is an output circuit of a controller.

21. The device according to claim 20, wherein the nonvolatile semiconductor memory device is of one of NAND and AND types.

22. An electronic card using a semiconductor integrated circuit device, the semiconductor integrated circuit device comprising:

a semiconductor region of a first conductivity type;

a first insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of a second conductivity type connected to an output terminal; and

a semiconductor region of the second conductivity type formed adjacent to the source/drain region on the semiconductor region of the first conductivity type and

connected to a gate of the insulated-gate field effect transistor.

23. An electronic card using a semiconductor integrated circuit device, the semiconductor integrated circuit device comprising:

a semiconductor region of a first conductivity type;

a first insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of a second conductivity type connected to an output terminal;

a second insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of the second conductivity type connected to a gate of the first insulated-gate field effect transistor to drive the first insulated-gate field effect transistor; and

a diode using the semiconductor region of the first conductivity type as one of an anode and cathode and having the other one of the anode and cathode formed on the semiconductor region of the first conductivity type and connected to the gate of the first insulated-gate field effect transistor, wherein

a distance from the source/drain region of the first insulated-gate field effect transistor to the other one of the anode and cathode is shorter than

a distance from the source/drain region of the first insulated-gate field effect transistor to the source/drain region of the second insulated-gate field effect transistor.

24. An electronic card using a semiconductor integrated circuit device, the semiconductor integrated circuit device comprising:

a semiconductor region of a first conductivity type;

a first insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of a second conductivity type connected to an output terminal;

a second insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of the second conductivity type connected to a gate of the first insulated-gate field effect transistor to drive the first insulated-gate field effect transistor; and

a third insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region connected to a gate thereof and a source/drain region connected to the gate of the first insulated-gate field effect transistor, wherein

a distance from the source/drain region of the

first insulated-gate field effect transistor to the source/drain region of the third insulated-gate field effect transistor which is connected to the gate of the first insulated-gate field effect transistor is shorter than a distance from the source/drain region of the first insulated-gate field effect transistor to the source/drain region of the second insulated-gate field effect transistor.

25. An electronic card using a semiconductor integrated circuit device, the semiconductor integrated circuit device comprising:

a semiconductor region of a first conductivity type;

a first insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of a second conductivity type connected to an output terminal;

a second insulated-gate field effect transistor formed on the semiconductor region of the first conductivity type and having a source/drain region of the second conductivity type connected to a gate of the first insulated-gate field effect transistor to drive the first insulated-gate field effect transistor; and

a bipolar transistor having a base formed of the semiconductor region of the first conductivity type, an emitter/collector region connected to the base and an

emitter/collector region connected to the gate of the first insulated-gate field effect transistor, wherein

a distance from the source/drain region of the first insulated-gate field effect transistor to the emitter/collector region of the bipolar transistor which is connected to the gate of the first insulated-gate field effect transistor is shorter than a distance from the source/drain region of the first insulated-gate field effect transistor to the source/drain region of the second insulated-gate field effect transistor.